

Having thus described the preferred embodiments, the invention is now claimed to be:

1. A document processing system comprising:
a controller, including a master clock and logic for generating a discrete clock synchronization interrupt signal;
a resource, including a slave clock related to operational timing of the
5 resource and circuitry for receiving and processing the discrete interrupt signal; and
a control bus, interconnecting the resource and the controller, for distributing the discrete interrupt signal.
- 10 2. The document processing system of claim 1 wherein the resource circuitry includes a processor for determining the compatibility of the slave clock with the master clock.
- 15 3. The document processing system of claim 1 wherein the resource circuitry includes a processor for adjusting the slave clock to provide for compatibility with the controller.
- 20 4. The document processing system of claim 3 wherein the compatibility between the resource and the controller provides hard real-time service.
5. The document processing system of claim 3 wherein the
compatibility between the resource and the controller is such that the slave clock is
synchronized to within one (1) clock cycle of the master clock.
- 25 6. The document processing system of claim 1, including a plurality of resources, each resource including a slave clock related to operational timing of the resource and circuitry for receiving and processing the clock synchronization interrupt signal, and wherein the control bus interconnects each resource with the controller thereby distributing the interrupt signal to each resource.

c) receiving the discrete interrupt signal at the resource and saving a first value of the slave clock;

d) sending a message from the resource to the controller via the network to request the value saved for the master clock;

5 e) sending the value saved for the master clock from the controller to the resource via the network;

f) receiving the value saved for the master clock at the resource;

g) saving a second value of the slave clock in the resource;

10 h) subtracting the first value from the second value to determine a slave clock difference value; and

i) adding the difference value to the value saved for the master clock to determine a synchronized value for the slave clock and setting the slave clock to the synchronized value.

15 14. The method of claim 13, the document processing system including a plurality of resources, each resource further including a slave clock related to operational timing of the resource, and the electrical interconnections further connecting each resource to the controller via the control bus and the network, wherein steps c) through i) are performed for each resource.

20 15. In a document processing system comprising a controller, the controller further including a master clock, a resource, the resource further including a slave clock related to operational timing of the resource, and electrical interconnections connecting the resource to the controller, the electrical interconnections further
25 comprising a control bus and a network, a method of synchronizing the slave clock with the master clock during steady state operation of the document processing system comprising the steps of:

a) saving a value of the master clock in the controller;

30 b) generating a discrete clock synchronization interrupt signal in the controller and distributing the discrete interrupt signal to the resource via the control bus;

c) receiving the discrete interrupt signal at the resource and saving a value of the slave clock;

d) sending a message from the resource to the controller via the network to request the value saved for the master clock;

5 e) sending the value saved for the master clock from the controller to the resource via the network;

f) receiving the value saved for the master clock at the resource; and

g) subtracting the value saved for the slave clock from the value saved for the master clock to determine an error value between the slave clock and the master
10 clock and using the error value in an adjustment algorithm to adjust the slave clock to be synchronized with the master clock.

16. The method of claim 15 wherein step g) results in synchronization of the slave clock to within one (1) clock cycle of the master clock.
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17. The method of claim 15 wherein steps a) through g) are performed periodically during steady state operation of the document processing system.

18. The method of claim 17 wherein the periodic interval for performing steps a) through g) during steady state operation of the document processing system is about two seconds.
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19. The method of claim 15, the document processing system including a plurality of resources, each resource further including a slave clock related to operational timing of the resource, and the electrical interconnections further connecting each resource to the controller via the control bus and the network, wherein
25 steps c) through g) are performed for each resource.

20. The method of claim 19 wherein step g) results in synchronization of each slave clock to within one (1) clock cycle of the master clock.
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21. An electrophotographic document processing system, operated in a xerographic environment, comprising:

a controller, including a master clock and logic for generating a discrete clock synchronization interrupt signal;

5 a plurality of resources, each resource including a slave clock related to operational timing of the resource and logic for receiving the discrete interrupt signal, processing the discrete interrupt signal, and synchronizing the slave clock with the master clock; and

10 electrical wiring interconnecting the resources and the controller for distributing the discrete interrupt signal to the resources.

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